IN THE CLAIMS:

The following is a complete listing of the claims in this application, reflects all changes currently being made to the claims, and replaces all earlier versions and all earlier listings of the claims:

Sub H-1

1-16 cancelled

17. (Currently amended): A memory controller comprising:

a converter section adapted to perform serial/parallel conversion of image data of "a" bit width inputted into image data of "a" x "2n"-bit width, where "a" is a natural number representing a size of the inputted bit width and "n" is a natural number;

a first FIFO (first-in-first-out) section adapted to temporarily store the image data of "a" x "2n"-bit width;

F1 cont

a frame memory section adapted to store image data of one frame; and

a second FIFO section adapted to temporarily store image data read out from said frame memory section,

wherein the image data is read out from said first FIFO section, written into said frame memory section, and read out from said frame memory section, at a rate that is half of a rate at which the image data is inputted into said first FIFO section, and,

wherein said first FIFO section is of a size suitable for storing image data, so that, within a period for inputting the image data into said first FIFO section to FULL capacity, writing the image data into said frame memory section, a plural times of reading the image data from said frame memory section, and executing a command of said frame memory section are conducted.

18. (Previously presented): A liquid crystal display comprising:

a liquid crystal panel;

a decoder adapted to convert an inputted image signal into an image signal adaptable to said liquid crystal panel,

wherein said decoder is provided with a memory controller according to Claim 17.